CLAIMS

What is claimed is:

1. A method for adjusting timing in a digital system, the method comprises the steps of:

dividing a data clock by a first value to produce a divided data clock;

dividing an analog front end clock by a second value to produce a divided analog front end clock;

comparing phase of the divided data clock with phase of the divided analog front end clock to produce a phase difference; and

adjusting the analog front end clock based on the phase difference to produce an adjusted analog front end clock.

2. The method of claim 1, wherein the adjusting further comprises:

filtering the phase difference to produce a control signal; and

controlling oscillation of a crystal based on the control signal, wherein the oscillation of the crystal provides the analog front end clock.

3. The method of claim 1 further comprises determining the first value based on at least one of: rate of the data, data transport protocol, and system configuration.

4. The method of claim 1 further comprises:

receiving data at a rate of the data clock; and

converting the rate from the data clock to a desired sample conversion rate, wherein the desired sample conversion rate is based on the adjusted analog front end clock and the data clock.

5. The method of claim 4 further comprises:

processing the data by a physical layer at the rate of the data clock to produce processed data; and

converting the rate of the processed data from the data clock to the desired clock rate.

6. A method for adjusting a sample rate conversion value, the method comprises the steps of:

sensing a data clock rate;

sensing an analog front end clock rate; and

adjusting the sample rate conversion value based on a function of the data clock rate and the analog front end clock.

7. The method of claim 6 further comprises:

obtaining a desired sample conversion rate; and

establishing a functional relationship between the data clock rate and the analog front end clock based on the desired sample conversion rate such that the resultant of the function is the sample rate conversion value.

8. The method of claim 7 further comprises:

dividing the data clock rate by a first value to produce a divided data clock;

dividing the desired sample conversion rate by a second value to produce a divided sample conversion rate;

comparing phase of the divided data clock with phase of the divided sample conversion rate to produce a phase difference; and

adjusting the analog front end clock rate based on the phase difference to produce an adjusted analog front end clock.

9. The method of claim 8 further comprises:

receiving data at the data clock rate; and

converting the rate from the data clock data to the desired sample conversion rate.

10. The method of claim 9 further comprises:

processing the data by a physical layer at the rate of the data clock to produce processed data; and

converting the rate of the processed data from the data clock to the desired clock rate.

11. A sample rate conversion clocking system comprises:

a first divider operably coupled to divide a data clock rate by a first value to produce a divided data clock rate;

a second divider operably coupled to divide an analog front end clock rate by a second value to produce a divided analog front end clock rate;

phase detector operably coupled to compare phase of the divided data clock rate to phase of the divided analog front end clock rate to produce a phase difference;

loop filter operably coupled to filter the phase difference to produce a control signal; and

crystal oscillator operably coupled to adjust oscillation of a crystal based on the control signal, wherein the oscillation of the crystal produces the analog front end clock rate.

12. The sample rate conversion clocking system of claim 11 further comprises:

value module operably coupled to sense the data clock rate and the analog front end clock rate, wherein the value module adjusts a sample rate conversion value based on a function of the data clock rate and the analog front end clock;

sample rate converter operably coupled to convert a rate of data from the data clock rate to a desired sample conversion rate based on the sample rate conversion value.

13. The sample rate conversion clocking system of claim 12 further comprises:

a physical layer operably coupled to process the data at the data clock rate to produce processed data, wherein the processed data is provided to the sample rate converter.

14. The sample rate conversion clocking system of claim 12, wherein the value module further comprises:

a register for storing a desired sample conversion rate; and

a functional module operably coupled to establish a functional relationship between the data clock rate and the analog front end clock rate based on the desired sample conversion rate such that the resultant of the function is the sample rate conversion value.

15. An apparatus for adjusting timing in a digital system, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

divide a data clock by a first value to produce a divided data clock;

divide an analog front end clock by a second value to produce a divided analog front end clock;

compare phase of the divided data clock with phase of the divided analog front end clock to produce a phase difference; and

adjust the analog front end clock based on the phase difference to produce an adjusted analog front end clock.

16. The apparatus of claim 15, wherein the memory further comprises operational instructions that cause the processing module to adjust the analog front end clock by:

filtering the phase difference to produce a control signal; and

controlling oscillation of a crystal based on the control signal, wherein the oscillation of the crystal provides the analog front end clock.

17. The apparatus of claim 15, wherein the memory further comprises operational instructions that cause the processing module to determine the first value based on at least one of: rate of the data, data transport protocol, and system configuration.

18. The apparatus of claim 15, wherein the memory further comprises operational instructions that cause the processing module to:

receive data at a rate of the data clock; and

convert the rate from the data clock to a desired sample conversion rate, wherein the desired sample conversion rate is based on the adjusted analog front end clock and the data clock.

19. The apparatus of claim 18, wherein the memory further comprises operational instructions that cause the processing module to:

process the data by a physical layer at the rate of the data clock to produce processed data; and

convert the rate of the processed data from the data clock to the desired clock rate.

20. An apparatus for adjusting timing in a digital system, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

sense a data clock rate;

sense an analog front end clock rate; and

adjust the sample rate conversion value based on a function of the data clock rate and the analog front end clock.

21. The apparatus of claim 20, wherein the memory further comprises operational instructions that cause the processing module to:

obtain a desired sample conversion rate; and

establish a functional relationship between the data clock rate and the analog front end clock based on the desired sample conversion rate such that the resultant of the function is the sample rate conversion value.

22. The apparatus of claim 21, wherein the memory further comprises operational instructions that cause the processing module to:

divide the data clock rate by a first value to produce a divided data clock;

divide the desired sample conversion rate by a second value to produce a divided sample conversion rate;

compare phase of the divided data clock with phase of the divided sample conversion rate to produce a phase difference; and

adjust the analog front end clock rate based on the phase difference to produce an adjusted analog front end clock.

23. The apparatus of claim 22, wherein the memory further comprises operational instructions that cause the processing module to:

receive data at the data clock rate; and

convert the rate from the data clock data to the desired sample conversion rate.

24. The apparatus of claim 23, wherein the memory further comprises operational instructions that cause the processing module to:

process the data by a physical layer at the rate of the data clock to produce processed data; and

convert the rate of the processed data from the data clock to the desired clock rate.